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| In re Application of: Chayan Mitra et al. | § | |
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| Serial No.: 10/732,839 | § | |
| | § | Examiner: Pizzaro Crespo, Marcus D. |
| Filed: December 10, 2003 | § | |
| For: STATIC INDUCTION TRANSISTOR | § | Atty. Docket: 134446-1/YOD GERD:0197 |

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January 30, 2005 — Lynda Howell
Date — Lynda Howell

## APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on November 22, 2005, and received by the Patent Office on November 28, 2005.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be necessary to advance prosecution of the present application, to Account No. 07-0868, Order No. 134446-1/YOD (GERD:0197).

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1. **REAL PARTY IN INTEREST**

The real party in interest is General Electric Company, the Assignee of the above-referenced application by virtue of the Assignment to General Electric Company by Chayan Mitra recorded at reel 014802, frame 0438, and recorded on December 10, 2003. Accordingly, General Electric Company, as the Assignee of the above-referenced application, will be directly affected by the Board's decision in the pending appeal.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. **STATUS OF CLAIMS**

Claims 1, 2 and 4-24 are currently pending, are currently under final rejection and, thus, are the subject of this Appeal.

4. **SUMMARY OF CLAIMED SUBJECT MATTER**

The present invention relates generally to the field of transistor switches. *See* Application, page 1, paragraph 1. More particularly, in certain embodiments, the invention relates to transistor switches used for high frequency and high power applications.

Typically, in power electronic applications, it is desirable to operate at high switching frequencies, especially in motor control and switch mode power supplies. For most of the high switching frequency applications in power circuits, it is generally required to use power devices with improved switching performance.

Gas discharge switches can be used for high frequency pulsed power applications. A few disadvantages of gas discharge switches are low repetition rates, short service lifetimes, weight and size. Such disadvantages can be overcome by using semiconductor

switches. Semiconductor based switches typically have lower power dissipation, longer life, fast turn-on and turn-off, high blocking voltage and improved current handling capability.

PiN bipolar rectifiers are typically used in power circuits for rectification and as anti-parallel diodes for switches such as insulated gate bipolar transistors (IGBT) and metal oxide semiconductor field effect transistors (MOSFET). One limitation of such devices operating at high switching frequencies is the reverse recovery process when a large reverse transient current flows through the device thereby increasing the diode power dissipation and producing an undesirable stress upon the power transistors operating in the circuits. Other rectifiers such as silicon Schottky rectifiers, on the other hand, exhibit poor, reverse blocking characteristics due to the Schottky barrier lowering effect and the large forward voltage drop that results when designed for high blocking voltage.

Power bipolar transistors are also used for high switching frequency and medium power applications. Most bipolar transistors are current controlled devices and a large reverse base drive current is often needed to obtain fast turn-off. Such devices are prone to second breakdown failure mode under simultaneous application of high current and high voltage as usually encountered in inductive power circuits.

Static induction transistors can also be used for high switching frequency applications. Charge transport in such transistors is due to majority carrier (for example electrons) flow through the channel, which is controlled by a channel potential barrier "induced" by a drain-source and a gate-source potential. Such transistors are typically vertical channel structures with uniform doping in the channel region. On proper scaling of such devices, large current handling capacity and low power dissipation in the on-state can be achieved. One problem with such transistors when made in silicon is their inability to withstand high blocking voltage because of low bandgap energy.

The Application is directed to providing a transistor switch that is suitable for operating in high switching frequency as well as withstanding high blocking voltages.

The Application contains two independent claims, namely claims 1 and 16, both of which are the subject of this Appeal. The subject matter of these claims is summarized below.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 1 relates to a transistor switch (e.g., 100) for a system operating at high frequencies. The transistor switch comprises a graded channel region (e.g., 140) between a source region (e.g., 110) and a drain region (e.g., 120), the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region. The graded channel comprises at least two doping levels. The switch further contains a gate region (e.g., 132) extending along a side wall of the graded channel, wherein the gate region is directly in contact with a gate contact. *See, e.g.,* Application, at page 4, paragraphs 12-15 and page 5, paragraph 17; *see also* FIG. 1.

With regard to the aspect of the invention set forth in independent claim 16, discussions of the recited features of claim 16 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 16 relates to a static induction transistor for a system operating at high frequencies. The static induction transistor comprises a graded channel region between a source region and a drain region. The graded channel region is configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region. The graded channel comprises at least two doping levels and the doping level at the source region is higher than doping level at the drain region. In

addition, the gate region extends along the sides of the graded channel, wherein the gate region is directly in contact with a gate contact. *See, e.g., id.* at page 4, paragraphs 12-15 and page 5, paragraphs 16- 17; *see also* FIG. 1 and FIG. 2.

This is a clear difference and distinction from the prior art, as discussed below.

## 5. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

**First Ground of Rejection for Review on Appeal:**

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,799,090 (hereinafter, "Nishizawa").

**Second Ground of Rejection for Review on Appeal:**

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 1, 2 and 4-24 under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Publication No. 2003/0178672 (hereinafter, "Hatakeyama") in view of U.S. Patent No. 5,945,701 (hereinafter, "Siergiej").

## 6. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Sections 102 and 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1, 2 and 4-24 are currently in condition for allowance.

**First Ground of Rejection**

Claim 1 recites a transistor switch for a system operating at high frequencies. The transistor switch comprises a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region. The graded channel comprises at least two doping levels. The transistor switch further includes a gate region extending along a side wall of the graded channel. The gate region is directly in contact with a gate contact.

The Examiner based the rejection on a comparison of the transistor switch in the present application with a tunnel injection controlling type semiconductor device controller disclosed by Nishizawa. Appellants have carefully reviewed the subject matter disclosed in Nishizawa and respectfully submit that Nishizawa does not teach the transistor switch recited in claim 1 for at least the reasons summarized below.

Appellants respectfully submit that the transistor switch recited in claim 1 is different from the tunnel injection controlling type semiconductor device controller disclosed by Nishizawa. In the present application, the transistor switch comprises a graded channel region configured for providing a low resistance to mobile negative charge carriers and a gate region extending along a side wall of a the graded channel, the gate region being in direct contact with a gate contact.

Sections at page 4, paragraphs 12-15 of the present application that relate specifically to the subject matter recited in claim 1.

> Static induction transistor 100 is shown comprising source region 110, drain region 120 and a gate region 130. The source region comprises source contact 111. Similarly the drain region and the gate region comprise drain contact 121 and gate contact 131 respectively. The source region and the drain region are negatively doped (n+) using mobile

> negative charge carriers whereas the gate region is positively doped (p+). In one embodiment, where the static induction transistor is designed using silicon carbide, the doping level of the source region and the drain region is 1018/cm3.
>
> As used herein, "adapted to", "configured" and the like refer to mechanical or structural connections between elements to allow the elements to cooperate to provide a described effect; these terms also refer to operation capabilities of electrical elements such as analog or digital computers or application specific devices (such as an application specific integrated circuit (ASIC)) that are programmed to perform a sequel to provide an output in response to given input signals.
>
> The static induction transistor further comprises graded channel 140 disposed between the source region and the drain region. The graded channel is configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region, wherein the graded channel comprises at least two doping levels. *As used herein, "graded channel" refers to a channel that has multiple doping levels.*
>
> In one embodiment, the graded channel is doped at two doping levels. The doping level of the channel near the source region is higher than the doping level at the drain region. The graded doping results in a lower electric field near the source region compared to the drain region. The low resistance allows the electrons in moving with higher velocity towards the drain and thereby reducing the electron transit time. In addition, by controlling the thickness of the drift layers in the graded channel, higher breakdown voltages can be achieved. (Emphasis added.)

Appellants respectfully submit that Nishizawa fails to disclose a graded channel that is configured for providing a low resistance to mobile negative charge carriers. Instead, Nishizawa discloses a transistor that has source region doped with a first conductivity type, and a drain region and channel region with the opposite conductivity

type. *See,* FIG. 2, column 3 and lines 19- 56. Nishizawa describes the structure as follows:

> In FIG. 2 is shown a basic sectional view of the transistor structure which is one of the embodiments of the present invention. Reference numeral 11 represents a p.sup.++ type source region; 14 an n.sup.+ type drain region; and 15 and 15' gate electrodes, respectively. These gate electrodes serve to control the potential distribution of the n.sup.+ type region 12 and of the n type region 13 which jointly constitute a current path via an insulation film 16. Regions 11' and 14' represent a source electrode and a drain electrode, respectively. The impurity concentrations and the sizes of the region 12 and the region 13 are designed so that these regions become almost or completely depleted in the operative state. The impurity concentrations of the respective regions are designed as follows, though they may vary depending on the distance between the gate regions. That is, 5 $X10^{19}$-1 X $10^{21}$ $cm^{-3}$ for the p++ type region 11; 5 X $10^{17}$-1 X $10^{19}$ $cm^{-3}$ for the n+ type region 12; 1 $X10^{14}$-1 X $10^{17}$ $cm^{-3}$ for the n type region 13 and 1 $X10^{18}$-5 X $10^{20}$ $cm^{-3}$ for the n+ type region. The impurity concentrations of the n+ type region 12 and of the n type region 13 are designed to be higher as the distance between the gate regions is set smaller, and also as the distance between the source region and the drain region is set smaller. In other words, the impurity concentrations of these two regions 12 and 13 can be set higher as the sizes of the respective constituting regions are designed finer. Therefore, as the sizes of the respective regions, and accordingly the size of the device as a whole, are reduced further, it becomes possible to obtain a higher tunnel current density. The gate-to-gate interval is, for example, from less than 2μm up to about 1000 A°. The distance between the source region and the drain region is set to be in the range from about 1000A° to about 2-3 μm. The thinner the insulation film 16 which is provided contiguous to the n+ type region 12 is, the more effectively will the gate voltage be applied to the n+ type region 12. Nishizawa, column 3, lines 19-56.

Clearly, with such doping patterns, the transistor switch disclosed by Nishizawa provides a path for both *negative carriers and positive carriers*, that is, electrons and holes respectively. Nishizawa fails to disclose a unipolar transistor switch that includes a *graded channel* for providing a low resistance path to mobile negative charge carriers. In addition, Nishizawa fails to disclose the gate region extending along the side wall of the graded channel and in direct contact with the gate contact. The gate electrode of the transistor, as disclosed by Nishizawa, controls the n+ type region 12 and the n type region 13 which jointly constitute a current path via an insulation film. *See*, FIG. 2, column 3 and lines 23-26.

Clearly, the gate electrode is *not in direct contact* with the gate region. Instead, the gate electrode is in contact with the insulation film. *See, e.g.*, FIG. 2, FIG. 4, FIG. 5, FIG. 7, FIG. 8 and FIG. 10. Nishizawa fails to disclose a gate region directly in contact with a gate contact.

Therefore, in view of the discussions hereinabove, Appellants submit that Nishizawa cannot anticipate claim 1 under 35 U.S.C. §102(b). Appellants respectfully request that the rejection of claim 1 and 16 and the claims depending therefrom be reversed.

**Second Ground of Rejection**

The rejection under 35 U.S.C. §103(a) for review may be analytically broken down into the following determinations, each of which will be discussed in detail below:

A. whether the combination of Hatakeyama and Siergiej teaches or motivates using a gate region extending along a side wall of a graded channel and a gate region directly in contact with a gate contact; and

B. whether the combination of Hatakeyama and Siergiej teaches or motivates using a graded channel region between a source region and a drain region,

configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region.

**A. Whether the combination of Hatakeyama and Siergiej teaches or motivates using a gate region extending along a side wall of a graded channel directly in contact with a gate contact.**

The Examiner rejected each of the independent claims 1 and 16 on the basis of Hatakeyama in view of Siergiej. Each of independent claims 1and 16 recites *a gate region extending along a side wall of the graded channel, wherein the gate region is directly in contact with a gate contact.*

Hatakeyama does not disclose, teach or suggest the gate region extending along the side wall of a graded channel and in direct contact with a gate contact. The high breakdown voltage semiconductor device, as disclosed by Hatekayama, includes a gate contact layer that is disposed within a gate region. The gate contact layer has a doping that is different from the gate region. The gate contact layer is in contact with the sidewall insulating film and the gate electrode :

> Moreover, sidewall insulating films 10a and 10b are selectively disposed in the gate layers 9 of the side surfaces 5a and 5b of the trench portion 5. As shown in FIGS. 2 and 3, these sidewall insulating films 10a and 10b are formed to surround outer peripheries of the plurality of insular convex portions. A sidewall insulating film 10c is also selectively disposed in the other side surface 5c of the trench portion 5'. As shown in FIGS. 2 and 3, the sidewall insulating film 10c is formed along the inside of an outer peripheral portion 3b of the device.
>
> Furthermore, a p-type third semiconductor layer (SiC layer) 12 is selectively disposed as a gate contact layer in the portion of the gate layer 9 in the bottom surface of the trench portion 5, and is exposed between the sidewall

insulating films (spacer layers) 10a and 10b. Hatakeyama, paragraphs 68 and 69.

Siergiej similarly fails to disclose, teach or suggest the gate region extending along the side wall of a graded channel and in direct contact with a gate contact. On the contrary, the gate region, as disclosed by Siergiej, is not formed within a graded channel but instead is formed *outside* the channel region. *See,* FIG. 12.

In short, neither reference teaches or suggests the gate region extending along the side wall of a graded channel and in direct contact with a gate contact. Consequently, the combination of Hatakeyama and Siergiej simply cannot suggest to one skilled in the art the gate region extending along the side wall of the graded channel and in direct contact with the gate contact as recited in claims 1 and 16.

In view of the forgoing considerations, the references fail to establish a *prima facie* case of obviousness of claims 1 and 16. These claims and the claims depending therefrom are therefore believed to be clearly patentable over the cited combination. Appellants request that the Board reverse the rejection at least for this first reason.

**B. Whether the combination of Hatakeyama and Siergiej teaches or motivates using a graded channel region between a source region and a drain region, configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region.**

Each of the independent claims 1and 16 recites *a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region.*

Hatakeyama does not disclose, teach or suggest using a graded channel region at all. The static induction transistor disclosed by Hatakeyama is not designed for graded doping. The channel disclosed by Hatakeyama has a single impurity concentration.

Siergiej similarly fails to disclose, teach or suggest the use of a graded channel. Siergiej, rather, teaches the use of first region or channel region, and a second region or a drift region. The channel region controls the flow of the majority carriers. The drift region is the region where the majority carriers drift towards the drain. *See*, FIG. 12, column 3, lines 22-32. As Siergiej explains:

> Layer 18 includes a first region 36 between the gates 22 and which extends from the source 16 to the bottom of the gate 22, or slightly below it, as indicated by the dotted line 37. This first region is where the gate controls the flow of majority carriers from the source and is termed herein the channel layer or channel region. A second region 38 extends from the first region to the drain 14 (to the top of buffer layer 17, if provided) and is the region where the majority carriers drift toward the drain and is termed herein the drift layer or drift region. Siergiej, column 3, lines 22-32; *see also,* Fig. 12.

Siergiej further discloses that the channel region has a first level of doping concentration and the drift region has a second level of doping concentration:

> The semiconductor body has a first region, a channel region, contiguous to said source and gates in which said gates control flow of said majority carriers from said source to said drain. The semiconductor body also has a second region, a drift region, which extends from said first region to said drain. The first and second regions have predetermined impurity atoms of a dopant added, with said first region having a higher average doping concentration than said second region. Siergiej, column 1, line 62 – column 2, line 3; *see also,* Fig. 12.

The channel region disclosed by Siergiej is not comparable to the graded channel recited by the Appellants in independent claims 1 and 16. The channel region disclosed by Siergiej comprises a single doping concentration. The graded channel of independent claims 1 and 16 clearly indicates that two or more doping levels are present. The mere fact that Siergiej discusses a static induction transistor switch with a channel region and a drift region of different concentration is not sufficient to provide a low resistance to mobile negative charge carriers using a graded channel.

The Examiner stated, "Siergiej, on the other hand, teaches that providing said graded channel region to Hatakeyama would achieve a uniform transconductance and voltage gain through the input signal range of the transistor (see, e.g., col.5/ll. 1-5)". This statement wrongly presupposes that either reference teaches or even suggests a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region. They do not. Consequently, the combination of Hatakeyama and Siergiej simply cannot suggest to one skilled in the art a graded channel region between a source region and a drain region, configured for providing a low resistance to mobile negative charge carriers, as recited in independent claims 1 and 16.

In view of the forgoing considerations, Appellants again submit that the references fail to establish a *prima facie* case of obviousness of claims 1 and 16. Claims 1 and 16 and the claims depending therefrom are therefore believed to be clearly patentable over the cited combination. Appellants request that the Board reverse the rejection at least for this additional reason.

**Conclusion**

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: 1/30/2006

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## 8. APPENDIX OF CLAIMS ON APPEAL

### Listing of Claims:

1. (previously presented) A transistor switch for a system operating at high frequencies, the transistor switch comprising:

a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region; wherein the graded channel comprises at least two doping levels; and

a gate region extending along a side wall of the graded channel; wherein the gate region is directly in contact with a gate contact.

2. (original) The transistor switch of claim 1, wherein doping level at the source region is higher than doping level at the drain region.

3. (canceled)

4. (original) The transistor switch of claim 1, wherein the transistor switch is implemented using a wide bandgap material with a high thermal conductivity.

5. (original) The transistor switch of claim 4, wherein the wide band gap material is selected from the group consisting of silicon carbide, gallium nitride, aluminum nitride, boron nitride, and diamond.

6. (original) The transistor switch of claim 1, wherein the graded channel comprises three doping levels.

7. (original) The transistor switch of claim 6, wherein the doping levels of the graded channel are 1015 electrons/cm3, 1016 electrons/cm3, and 1017 electrons/cm3.

8. (original) The transistor switch of claim 1, wherein the doping level of the source region and the drain region is 5 x 1018 electrons/cm3 respectively.

9. (original) The transistor switch of claim 1, wherein the doping level of the gate region is 5 x 1018 holes/cm3.

10. (original) The transistor switch of claim 1, wherein the transistor switch operates at a frequency of at least 1MHz.

11. (original) The transistor switch of claim 1, wherein the transistor switch operates at a frequency of more than 68 MHz.

12. (original) The transistor switch of claim 1, wherein the breakdown voltage of the transistor switch is more than 60 Volts.

13. (original) The transistor switch of claim 12, wherein the breakdown voltage of the transistor switch is 210 Volts.

14. (original) The transistor switch of claim 1, wherein the transistor switch is implemented in high power generating systems.

15. (original) The transistor switch of claim 1, wherein the transistor switch comprises a static induction transistor.

16. (previously presented) A static induction transistor for a system operating at high frequencies, the static induction transistor comprising:

a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region; wherein the graded channel comprises at least two doping levels, wherein doping level at the source region is higher than doping level at the drain region; and wherein a gate region extends along the sides of the graded channel, wherein the gate region is directly in contact with a gate contact.

17. (original) The static induction transistor of claim 16, wherein the graded channel comprises three doping levels.

18. (original) The static induction transistor of claim 17, wherein the doping levels of the graded channel are 1015 electrons/cm3, 1016 electrons/cm3, and1017 electrons/cm3.

19. (original) The static induction transistor of claim 16, wherein the doping level of the source region and the drain region is 5 X 1018 electrons/cm3 respectively.

20. (original) The static induction transistor of claim 16, wherein the doping level of the gate region is 5 X 1018 holes/cm3.

21. (original) The static induction transistor of claim 16, wherein the static induction transistor operates at a frequency of at least 1MHz.

22. (original) The static induction transistor of claim 16, wherein the static induction transistor operates at a frequency of more than 68 MHz.

23. (original) The static induction transistor of claim 16, wherein the breakdown voltage of the static induction transistor is more than 60 Volts.

24. (original) The static induction transistor of claim 23, wherein the breakdown voltage of the static induction transistor is 210 Volts.

## 9. APPENDIX OF EVIDENCE

None.

## 10. APPENDIX OF RELATED PROCEEDINGS

None.